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Avilla, IN 46710
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FACSIMILE COVER LETTER

March 9, 2006

To: Latrice Sims (571-273-6500)

Company: Deposit Accounts, U.S. Patent and Trademark Office

From: Todd T. Taylor

RE: Refund to Deposit Account No. 200095
Our ref: LII0039.US/ LE9-98-030 U.S. Serial No. 09/226,971

Comments:

Total number of pages, including this page: 29

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PATENT MAINTENANCE DIVISION

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US PATENT & TRADEMARK OFFICE

TAYLOR & AUST, P.C.
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**ROGER M. RICKERT

**OF COUNSEL

March 9, 2006

Via facsimile
571-273-6500

Commissioner for Patents and Trademarks
Deposit Accounts
Mail Stop 16
PO Box 1450
Alexandria, VA 22313-1450

ATTN: Latrice Sims

RE: Refund to Deposit Account No. 200095
Our file ref: LII0039.US/ LE9-98-030, Serial No. 09/226,971

Dear Ms. Sims:

Enclosed herewith please find a copy of the monthly Statement of Deposit Account dated December 2005.

As shown on the attached Monthly Statement of Deposit Account, Deposit Account No. 200095 was debited a total amount of $200.00 in association with U.S. Patent Serial No. 09/226,971. In particular, the Monthly Statement of Deposit Account indicated that the total amount of $200.00 for an extra independent claim was not included. However, on November 18, 2005 an amendment was submitted with no change to the number of claims since the last amendment which was filed on May 14, 2001. Copies of these documents are enclosed for your review. Thus, it is requested that the $200.00 taken out of the deposit account on December 2, 2005, for an extra independent claim be refunded.

Accordingly, it is respectfully requested that Deposit Account No. 200095 be credited in the amount of $200.00 for this error.

If you have any questions, please do not hesitate to telephone the undersigned.

Sincerely,

Todd T. Taylor

TTT/mb
Encs: Copy of Monthly Statement of Deposit Account
Document filed with the USPTO as mentioned

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UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MONTHLY STATEMENT OF DEPOSIT ACCOUNT

To replenish your deposit account, detach and return top portion with your check. Make check payable to Director of Patents & Trademarks.

TAYLOR & AUST, P.C.
TODD TAYLOR
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FINA

Account No.
200095
Date
12-30-05
Page
1

PLEASE SEND REMITTANCES TO:
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12	2	05	1	10165237	XYZ claims	PDL0047.US	2202	250.00	1861.00
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Michael A. Marra et al.
Serial No.: 09/226,971
Filed: January 8, 1999
Title: METHOD OF REGULATING A TARGET SYSTEM USING A FREQUENCY COMPARISON OF FEEDBACK AND REFERENCE PULSE TRAINS

Group: 2121

Examiner: B. Garland

AMENDMENT TRANSMITTAL SHEET

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as follows:

	CLAIMS AS AMENDED					
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
TOTAL CLAIMS	8	MINUS	20	0	x $25 x $50	0.00
INDEPENDENT CLAIMS	4	MINUS	4	0	x $100 x $200	0.00
	FEE FOR MULTIPLE CLAIMS $130/$260					
	TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$0.00

[ ] A check in the amount of $0.00 is enclosed to cover the additional fees. (Check**)
[ ] A check in the amount of $_ to cover the Extension fee for response within the ( ) month is enclosed.
[ ] Applicants authorize the additional fees in the amount of $_* be charged to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Respectfully submitted,

Todd T. Taylor
Attorney for Applicant

Enc: Return Postcard

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Telephone: 260-897-3400
Facsimile: 260-897-9300

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)
Michael A. Marra et al.	) Group: 2121
Serial No.: 09/226,971	)
Filed: January 8, 1999	)
Title: METHOD OF REGULATING A TARGET	)
SYSTEM USING A FREQUENCY	)
COMPARISON OF FEEDBACK AND	)
REFERENCE PULSE TRAINS	) Examiner: B. Garland

AMENDMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Decision on Appeal dated September 20, 2005, Applicants hereby submit the following Amendment.

The following sections are included herewith:

- Amendment(s) To The Claims
- Remarks

PATENT

AMENDMENT(S) TO THE CLAIMS

1. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal; and

providing said control signal as an input to said target system.

2. (original) The method of regulating a target system of claim 1, wherein said comparing step comprises substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train.

3. (original) The method of regulating a target system of claim 2, wherein said step of generating said control signal comprises the substep of generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train.

4. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison without regard to phase locking said feedback pulse train to said reference signal, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

5. (original) The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substep of generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals.

6. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison <u>without regard to phase locking said feedback pulse train to said reference signal</u>, said generating step including the

substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being

dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. (currently amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison <u>without regard to phase locking said feedback pulse train to said reference signal</u>, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1 when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.

8. (original) The method of regulating a target system of claim 1, wherein said frequency of said feedback pulse train varies with time.

PATENT

REMARKS

Claims 1-8 are pending and rejected in this application pursuant to a decision by The Board of Patent Appeals and Interferences dated September 20, 2005. Claims 1, 4, 6 and 7 are amended hereby.

Responsive to the rejection of claim 1 based upon Motorola Reference Data Sheet for the MC4344/MC4044 Phase-Frequency Detector (Motorola), Applicants have amended claim 1 and submit that claim 1 and claims 2, 3, 5 and 8 depending therefrom are now in condition for allowance.

Motorola indicates that the circuit is useful for a range of phase-locked loop applications. Phase detector #1 is intended for uses in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired (page 6-20). Relative to phase detector #1, loop lock-up occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on the reference input and the variable or feedback input coincide (page 6-22). Relative to phase detector #2 there is a quadrature relationship between the reference input and the variable or feedback input. Any deviation from a 50% duty cycle on the inputs appear as a phase error (page 6-23).

In contrast claim 1, as amended, recites in part:

> generating a control signal dependent upon said comparison <u>without regard to phase locking</u> said feedback pulse train to said reference signal;

(Emphasis added). Applicants submit that such an invention is neither taught, disclose nor suggested by Motorola or any of the other cited references, alone or in combination, and has distinct advantages thereover.

Motorola discloses a phase locking circuit that locks the phase of an input signal to that of a reference signal or to a quadrature lock, which causes the output to be locked at a 90° phase shift from the reference signal. Applicants invention does not determine a phase error and

regulates a target system without regard to any phase locking. In contrast Motorola discloses the phase locking of an input signal to a reference signal. Therefore Motorola fails to disclose, teach or suggest generating a control signal dependent upon a comparison without regard to phase locking the feedback pulse train to the reference signal, as recited in claim 1.

An advantage of Applicants' invention is that less space is needed for the frequency comparison circuitry than the phase detection circuitry of the reference, since comparison of the relative phases of two signals and the generation of a phase error correction signal are not necessary. Another advantage of Applicants' invention is that phase differences are not detected and not corrected; as a result thereof the circuitry of Applicants' invention has a reduced cost of implementation. Another advantage of Applicants' invention is that there is less electrical noise in the control system than is present in phase detection and control circuits. For the foregoing reasons, Applicants submit that claim 1 and claims 2, 3, 5 and 8 depending therefrom are now in condition for allowance, which is hereby respectfully requested.

Even though the Decision of the Appeal indicated that the application of the Motorola reference was only relative to independent claim 1, Applicants have additionally amended claims 4, 6 and 7 to include the phrase, "without regard to phase locking said feedback pulse train to said reference signal" in a manner similar to that incorporated into claim 1. For the same reasons, stated above relative to claim 1, Applicants submit that claims 4, 6 and 7 are additionally now in condition for allowance, which is hereby respectfully requested.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the amended claims. The pending claims are therefore in condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

PATENT

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorizes that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (260) 897-3400.

Respectfully submitted,

Todd T. Taylor
Registration No. 36,945

Attorney for Applicant

TTT6/dc

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Facsimile: 260-897-9300

Enc.: Return postcard

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on: November 18, 2005

Todd T. Taylor, Reg. No. 36,945
Name of Registered Representative

Signature

November 18, 2005
Date

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Michael A. Marra et al.
Serial No.: 09/226,971
Filed: January 8, 1999
Title: METHOD OF REGULATING A TARGET SYSTEM USING A FREQUENCY COMPARISON OF FEEDBACK AND REFERENCE PULSE TRAINS

Group: 2121

Examiner: B. Garland

AMENDMENT TRANSMITTAL SHEET

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as follows:

CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
TOTAL CLAIMS	8	MINUS	20	0	x $ 9 x $18	0.00
INDEPENDENT CLAIMS	4	MINUS	3	1	x $40 x $80	80.00
	FEE FOR MULTIPLE CLAIMS $130/$260					
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$80.00

[ ] Verified Statement claiming small entity status is enclosed, if not filed previously.
[X] A check in the amount of $ 80.00 is enclosed to cover the additional fees. (Check 6794)
[ ] A check in the amount of $_ to cover the Extension fee for response within the ( ) month is enclosed.

Respectfully submitted,

Todd T. Taylor
Attorney for Applicant

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PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Michael A. Marra et al. Serial No.: 09/226,971 Filed: January 8, 1999 Title: METHOD OF REGULATING A TARGET SYSTEM USING A FREQUENCY COMPARISON OF FEEDBACK AND REFERENCE PULSE TRAINS	Group: 2121 Examiner: B. Garland

AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive to the Office Action dated February 14, 2001, Applicants hereby submit the following Amendment.

Attached hereto as "ATTACHMENT A" is a marked-up copy showing the changes made to the above-identified patent application by the present Amendment.

IN THE CLAIMS

Please substitute the following amended claims 4, 6 and 7 for original claims 4, 6 and 7:

4. (Amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

6. (Amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. (Amended) A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1 when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.

REMARKS

Claims 1-8 are pending in this application. Claims 1-3, 5 and 8 are rejected; and claims 4, 6 and 7 are objected to in this application. Keeping in mind the Examiner's recommendation to rewrite claims 4, 6 and 7 in independent form, claims 4, 6 and 7 are amended hereby.

Responsive to the rejection of claims 1 and 8 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,212,434 (Hsieh) Applicants respectfully traverse the rejection.

Hsieh discloses a phase-locked step motor speed servo controller, including motor 50, speed detector 60 and phase detector 10. Phase detector 10 having a first input port V and a second input port R. First input port V is connected to the output of speed detector 60 to receive feedback signal $P_1(t)$ having phase θ_1 and second input port R is connected to reference signal $P_2(t)$ whose frequency is f_2 and phase is θ_2. The difference between the phase θ_1 of feedback signal $P_1(t)$ and phase θ_2 of reference signal $P_2(t)$ is the phase error θ_e ($\theta_e = \theta_1 - \theta_2$). Phase error θ_e will cause up-down counter 22 to increase or decrease proportional to $\theta_e / 2\pi$, the count of which is utilized to alter output voltage V_o, which is proportional to θ_e as shown in Fig. 5. V_o increases if θ_e indicates a phase lag, causing an increase in the rate of pulses sent to motor 50 in order to increase the speed of motor 50. Conversely, V_o decreases if θ_e indicates a phase lead, causing a decrease in the rate of pulses sent to motor 50 in order to decrease the speed of motor 50.

In contrast, claim 1 recites in part:

> generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;
>
> providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;
>
> comparing said frequency of said reference pulse train with said frequency of said feedback pulse train.

(Emphasis added) Applicants submit that such structure is neither taught, disclosed nor suggested by Hsieh or any of the other cited references, alone or in combination, and includes distinct advantages thereover.

Hsieh teaches the use of the comparison of the phase of a signal generated by a speed detector to the phase of a reference signal to adjust the input to a motor. However, Hsieh fails to disclose or suggest the generating of a reference pulse train, which is not dependent on the phase of the reference signal, and using the reference pulse train and the feedback pulse train to generate control signals for the correction of the speed of a motor. Accordingly, Applicants submit that claim 1, and claim 8 depending therefrom, are now in condition for allowance, which is hereby respectfully requested.

Claims 2, 3 and 5 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,212,434 (Hsieh) in view of either U.S. Patent No. 4,494,509 (Long) or U.S. Patent No. 6,043,695 (O'Sullivan). However, claims 2, 3 and 5 depend from claim 1 which has been placed in condition for allowance for the reasons given above. Accordingly, Applicants submit that claims 2, 3 and 5 are now in condition for allowance, which is hereby respectfully requested.

For the foregoing reasons, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the claims as amended. The pending claims are therefore in condition for allowance, and Applicants respectfully request withdrawal of all rejections and allowance of the claims.

In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicants hereby conditionally petition therefor and authorize that any charges be made to Deposit Account No. 20-0095,

PATENT

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (219) 897-3400.

Respectfully submitted,

Todd T. Taylor
Registration No. 36,945

Attorney for Applicant

TTT6/ar

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Title: METHOD OF REGULATING A TARGET SYSTEM USING A FREQUENCY COMPARISON OF FEEDBACK AND REFERENCE PULSE TRAINS PATENT
Application Serial No.: 09/226,971 Group: 2121 Examiner: B. Garland

ATTACHMENT A:
MARKED-UP COPY SHOWING AMENDMENTS

IN THE CLAIMS

4. (Amended) [The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substeps of:]

A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train;

substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first proportional clock CP1 at a frequency fP1 when said digital signals of said proportional error pulse train are in a high state;

resetting said first proportional clock CP1 to zero when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first proportional clock CP1 into a second proportional clock CP2 each time said first proportional clock CP1 transitions from a high state to a low state;

counting down from said loaded current value with said second proportional clock CP2 at a frequency fP2 until a zero value is reached; and

determining a proportional error term representing a time average of a signal which is held high while said second proportional clock CP2 is in a high state and held low while said second proportional clock CP2 is in a zero state, said control signal being dependent upon said proportional error term; and

providing said control signal as an input to said target system.

6. (Amended) [The method of regulating a target system of claim 5, wherein said step of generating said control signal comprises the further substeps of:]

A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train

with a leading edge of each digital signal in said feedback pulse train:

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

generating an error direction pulse train including a plurality of digital signals, each said digital signal representing a directionality of said error between said corresponding pair of aligned digital signals;

counting up from zero with a first integral clock CI1 at a frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are simultaneously in a high state;

counting down with said first integral clock CI1 at said frequency fI1 when said digital signals of said proportional error pulse train are in a high state and said digital signals of said error direction pulse train are in a low state;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state;

loading a current value of said first integral clock CI1 into a second integral clock CI2 each time said first integral clock CI1 transitions from a high state to a low state;

counting down from said loaded current value with said second integral clock CI2 at a frequency fI2 until a zero value is reached; and

determining an integral error term representing a time average of a signal which is held high while said second integral clock CI2 is in a high state and held low while said second integral clock CI2 is in a zero state, said control signal being dependent upon said integral error term; and

providing said control signal as an input to said target system.

7. (Amended) [The method of regulating a target system of claim 3, wherein said step of generating said control signal comprises the further substeps of:]

A method of regulating a target system, comprising the steps of:

providing a reference signal;

generating a plurality of digital signals defining a reference pulse train with a frequency dependent upon said reference signal;

providing a target system to be regulated, said target system having an output in the form of a plurality of digital signals defining a feedback pulse train having a frequency;

comparing said frequency of said reference pulse train with said frequency of said feedback pulse train, and substantially aligning a leading edge of each digital signal in said reference pulse train with a leading edge of each digital signal in said feedback pulse train;

generating a control signal dependent upon said comparison, said generating step including the substeps of:

generating a proportional error pulse train including a plurality of digital signals, each said digital signal representing an error between a corresponding pair of aligned digital signals of said reference pulse train and said feedback pulse train;

counting up from zero with a first derivative clock CD1 at a frequency fD1

when said digital signals of said proportional error pulse train are in a high state;

subtracting a current state of said first derivative clock CD1 from a current state of a register R each time said first derivative clock CD1 transitions from a high state to a low state;

loading said subtracted state into a second derivative clock CD2;

loading said current state of said first derivative clock CD1 into said register R;

resetting said first derivative clock CD1 to zero;

counting down with said second derivative clock CD2 at a frequency fD2 after said subtracted state is loaded therein;

maintaining said first integral clock CI1 at a current value when said digital signals of said proportional error pulse train are in a low state; and

determining a derivative error term representing a time average of a signal which is held high while said second derivative clock CD2 is in a high state and held low while said second derivative clock CD2 is in a zero state, said control signal being dependent upon said derivative error term; and

providing said control signal as an input to said target system.

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APPLICANT: Michael A. Marra et al.
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